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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/064,441	07/15/2002	Michael J. Lercel	BUR920010177	5777

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EXAMINER	
ROSASCO, STEPHEN D	

ART UNIT	PAPER NUMBER
1756	

DATE MAILED: 03/17/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/064,441	LERCEL ET AL.	
	Examiner	Art Unit	
	Stephen Rosasco	1756	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 February 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *15 July 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *7/15/02*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Detailed Action

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-11 are rejected under 35 U.S.C. 102(b) as being anticipated by Levinson et al. (6,098,408).

The claimed invention provides a method and apparatus that minimizes the destructive effects of non-reflected energy during lithography. More specifically, a cooling system is localized within the mask. In one example, a cooling module is integrated into the EUV mask. The cooling module may be thermoelectric.

The EUV mask comprises a substrate structure as a base for a reticle, a cooling layer, which is formed on the substrate structure and a planarizing layer deposited on the cooling layer. In another example, a cooling channel is formed within the mask.

In semiconductor lithography, and more specifically, extreme ultraviolet lithography (hereinafter "EUVL"), the desired pattern is imaged on top of a reflective subsirate through an absorber layer by a mask or reticle. The reflective layer, however, has about a 70% reflectivity. Thus, the remaining non reflected energy, about 30%, is absorbed in the reflective substrate. Accordingly, during exposure, a large amount of heat is absorbed in the reticle substrate. The non-reflected energy in the reticle results in the reticle being heated, which causes the reticle to distort. Since the reticle illumination is non-telecentric, the distortion leads to large image placement variations on the wafer.

To overcome these distortions and variations, careful control of the reticle flatness and temperature, during the lithography, is required. Traditionally. a substrate material with a very

low coefficient of thermal expansion and with a low flatness value is utilized, which results in minimizing the adverse effect of the non-reflected energy. However, materials that meet these standards are difficult to manufacturer and/or expensive.

Levinson et al. teach a system for regulating reticle temperature in an EUV mask, comprising: a plurality of thermoelectric coolers operatively coupled to a reticle;

a power source for powering the plurality of thermoelectric coolers; and

a processor operatively coupled to the power source, the processor mapping the reticle into a plurality of grid blocks, each thermoelectric cooler being associated with a respective grid block of the plurality of grid blocks, the processor controlling the thermoelectric coolers so as to selectively regulate temperature of portions of the reticle.

And further including a thermally conductive material interposed between at least one of the thermoelectric coolers and the reticle.

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Levinson et al. (6,098,408) or Macris (6,686,532) in view of Geusic et al. (6,496,370).

The description of the claimed invention and the cited art to Levinson et al. is included here as stated above.

Macris teaches a heat dissipating IC device comprising: at least one IC die comprising a semiconductor substrate including at least one circuitry layer on at least one substrate face; at least one thermoelement couple, said couple comprised of the semiconductor substrate and at least one dissimilar conductor electrically bonded to the semiconductor substrate thereby creating junctions; and said thermoelement couple comprises at least one heat absorbing junction and at least one heat rejecting junction wherein the heat absorbing junction is positioned near the center of the substrate face and the heat rejecting junction is positioned near the perimeter of the substrate face.

And wherein the dissimilar conductor comprises more than one layer.

The teachings of Levinson et al. or Macris differ from those of the applicant in that the applicant teaches the use of cooling channels in the substrate for passing liquid through in order to cool the mask during exposure.

Geusic et al. teach an electronic system module, comprising: a semiconductor wafer having first and second opposing surfaces and having cooling channels passing through the wafer between the first and second opposing surfaces; wherein the cooling channels are filled with a liquid. It would have been obvious to one having ordinary skill in the art to take the teachings of Levinson et al. or Macris and combine them with the teachings of Geusic et al. in order to make the claimed invention because it would be obvious to incorporate any known cooling method that is available.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Stephen Rosasco whose telephone number is 571-272-1389. The examiner can normally be reached on M-F from 9 to 5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark Huff, can be reached on 571-272-1385. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

For general Information call (571-272-1700).

S. Rosasco
Primary Examiner
Art Unit 1756

S.Rosasco
3/6/04